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An Overview on Strategies to Perform VLSI Testing Productively Utilizing BIST

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----------**ABSTRACT**----------

A survey on techniques to perform VLSI Testing efficiently using BIST explores various methodologies to enhance Very Large-Scale Integration (VLSI) testing through Built-In-Self-Test (BIST) mechanism. The research delves into the significance of BIST controllers, such as the utilization of Low-Feedback Shift Registers (LFSR) for efficient testing. It also addresses the critical challenge of reducing test power in low-power VLSI circuits, emphasizing the need for innovative techniques to mitigate excessive power consumption during testing processes. Furthermore, the paper highlights the evolution of BIST applications in VLSI and System-on-Chip (SoC) testing, showcasing the growing importance of BIST for fault detection in modern electronic devices. Additionally, the study focuses on the design of Logic BIST structures, emphasizing the role of components like Test Pattern Generators, Response Analyzers, and Comparators in enhancing chip testing efficiency.

Keywords: **BIST, Low-Feedback Shift Registers (LFSR), SoC testing, TPG**

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1. INTRODUCTION

The complexity and thickness of integrated circuits (ICs) continue to rise with the advancement of Very-Large-Scale Integration (VLSI) technology, making the testing of these devices more and more demanding. Effective testing methods are essential to ensuring the reliability and use of VLSI circuits, since even small flaws can lead to serious problems with operation or total device disappointment. By giving ICs the ability to test themselves, Built-In-Self-Test (BIST) has emerged as a crucial tactic in responding to these developments, increasing test efficacy and reducing dependency on external testing hardware. This paper gives an outline of the various methodologies utilized to perform VLSI testing gainfully utilizing BIST. We will investigate the crucial ideas of BIST, including its engineering and functional standards. Additionally, the study will examine how BIST and Design for-testability (DFT) approaches reconcile, since these approaches combined aid in the early identification of flaws and improve the overall testability of complex integrated circuits. We aim to demonstrate the practicality of BIST in verifiable scenarios and demonstrate how it contributes to reducing test time, lowering costs, and increasing shortcoming inclusion through the analysis of contextual analyses and pragmatic applications.

2. BIST

The development of semiconductor manufacturing technology has presented a number of testing issues for the fabrication and use of very-large-scale integration (VLSI) circuits, including wafer probe, wafer sort, pre-ship screening, and incoming test of circuits and chips, testing-built boards, testing the system, routine maintenance, testing repairs, etc.[1]. The conventional methods of testing digital circuits by using Automatic Test Pattern Generation (ATPG) software to identify individual faults have grown very costly and are unable to offer deep submicron or nanometer designs, from the chip level to the board and system levels, with a high enough fault coverage. Adding built-In Self-Test (BIST) capabilities to a digital circuit during the design phase is one way to address these testing issues. Logic BIST circuits are incorporated in the chip or located elsewhere on the same board as the chip. They are responsible for creating test patterns and analyzing the functional circuitry's output replies. For the purpose of verifying random logic, BIST approaches fall into two main categories: (1) online BIST and (2) offline BIST.

When the functional circuitry is operating normally, online BIST is executed. Either concurrent or non-concurrent operation is possible. Concurrent online BIST allows testing to happen at the same time as regular functional operation. Functional circuitry is typically accomplished using duplication and comparison or coding approaches. When a temporary or intermittent error is identified, the system will either immediately fix it, restore the system to its previously saved states, and carry out the action again, or it will create an interrupt signal in the event that failures occur repeatedly. Testing is done while the functional circuitry is in idle mode in non-concurrent online BIST.

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Usually, diagnosis firmware routines (microcode) or diagnosis software routines (macrocode) are executed to do this. Any moment during the test procedure, it can be stopped to allow for the return of regular business. When the functional circuitry is not operating in the typical manner, offline BIST is executed. Although this method does not identify problems in real time, it is commonly employed in the industry to verify product quality by checking the functioning circuitry at the system, board, or chip level.

3. ARCHITECTURE OF BIST

The below Figure shows a representative architecture[2] of the BIST circuitry as it might be integrated into the CUT.

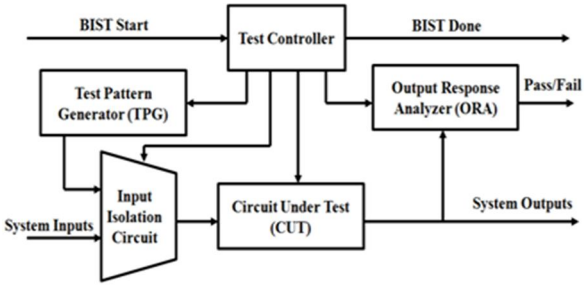

Figure 1: Architecture of BIST[2]

The Test Pattern Generator (TPG) and the Output Response Analyzer (ORA) are the two key components. The ORA condenses the CUT's output replies into a Pass/Fail indicator, whereas the TPG generates a series of patterns for testing the CUT [2]. The input isolation circuitry and the test controller, also known as the BIST controller, are the other two features required for the BIST to be used at the system level.

4. LITERATURE SURVEY

Kumar M, et. al. [2] emphasized the significance of memory testing for System-on-Chip (SOC) designs and the growing use of BIST, such as Built-in Self-Diagnosis (BISD) schemes, for memory testing. The proposed BIST structure can detect and diagnose faults in both interconnect resources and CLBs, with the ability to uniquely identify multiple faults in interconnects, including various types of faults like short-open, delay faults, and stuck-at faults. Memory testing involves techniques like test data compression, fault syndrome analysis, and redundancy repair to enhance memory yield and ensure effective testing and diagnosis of non-volatile memory failures.

Peng Z, et. al.[3] Introduced a novel method of low-power test vector generation based on LFSR reseeding, addressing the challenge of high-power consumption during chip testing. Deep analysis of the relationship between test vectors and test vector seeds in LFSR reseeding technology leads to the proposal of a model for optimizing dynamic test power consumption based on Hamming distance sorting test vector seeds [3]. Experimental simulations based on ISCAS85 and ISCAS89 demonstrate significant improvements, including a reduction in test vector seed storage bits, increased fault coverage, reduced circuit area overhead, and decreased dynamic test power consumption. By selecting the C499 circuit for BIST implementation and conducting feature analysis, the paper effectively proves the efficiency of the proposed low-power test vector generation method.

Menbari A, et. al.[4] Suggested the concurrent BIST design in the paper which enables testing to take place concurrently with regular operations. Concurrent Test Latency (CTL), or the number of cycles required to finish testing, is an important characteristic. The goal of the suggested design is to reduce CTL. The majority of current techniques include large combinational circuits, excessive hardware overhead, or unfeasible CTL. These problems are well handled by the suggested design. The suggested design primarily consists of LFSRs and a minimal decoding combinational module, which minimizes hardware overhead [4].
The suggested approach is flexible enough to accommodate varying circuit requirements since it can be used to tune and alter hardware overhead and CTL. The suggested design achieves a 10% decrease in hardware overhead for large-scale circuits while minimizing CTL when compared to the most effective current approach. Experiments demonstrate that the suggested design is versatile for a range of applications, as it can be tuned between CTL and hardware overhead. The suggested approach considerably lowers CTL in comparison to earlier approaches where hardware overhead and CTL are both equally relevant, with just a minor increase in hardware overhead for large- and very large-scale circuits.

W. Waller, et. al.[5] Proposed an algorithm for designing convolved LFSR/SR for pseudo-exhaustive testing (PET) to reduce hardware overhead and test set lengths. An efficient search is conducted to minimize the constraint on the size of the shift register segment and limit the number of feed forward stages to two at most. The algorithm generates multiple solutions for each case, allowing the selection of minimal hardware solutions. A new test pattern generator (TPG) for PET is introduced, bridging the gap between convolved LFSR/SR and permuted LFSR/SR, considered optimal for test set lengths and hardware overhead. The paper presents new algorithms and generators for pseudo-exhaustive testing, including NEWCONV, NEWGEN, and PETPG, designed for combinational benchmark circuits. Results show that the new convolved LFSR/SR design (NEWCONV) consistently outperforms existing algorithms in terms of hardware overhead and runtime.

Ahmed M, et. al.[6] Discussed a unique approach for fault identification and repair in Static Random-Access Memory (SRAM) that combines Bit-Swapping-based Linear Feedback Shift Register (BSLFSR) with Deep Q-learning (DQL). The suggested hybrid method, called DQL-BSLFSR, makes use of spare rows and columns for repair and redundancy analysis to identify problematic cells. DQL

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is used for fault injection and detection. Faulty addresses discovered during memory testing are stored by redundancy management logic, and when read and write operations coincide, the BSLFSR-BISR technique initiates repair. In comparison to earlier approaches, the suggested DQL-BSLFSR-FD model exhibits reduced power consumption and enhanced operating frequency, highlighting its effectiveness in memory defect recovery. Through Verilog simulation, the design and implementation of the suggested BIST and Built-In Self-Repair methods were verified on FPGA, demonstrating the methodology's usefulness. The DQL-BSLFSR-FD model outperforms conventional FPGA-based fault detection techniques in terms of size, power consumption, and latency reduction, according to a comparison in the study.

Shrivastava S, et. al.[7] Explored BIST testing techniques for fault detection and coverage. Various BIST architectures were evaluated based on hardware overhead. Window vector monitoring And Input vector controlling parallel BIST technology are the methods used. Proposed concurrent BIST technique has lower hardware overhead than others. Simulation results show successful BIST architecture with minimized slice register and this scheme has lower hardware overhead compared to other BIST techniques.

Jahanirad H, et. al.[8] Provided a method for testing Look-Up Tables (LUTs) in SRAM-based FPGAs with an emphasis on locating single stuck-at defects in the LUTs of each Configurable Logic Block (CLB) using Built-in Self-Test (BIST). To generate exhaustive test vectors, a 4-bit counter is utilized, while a combination of XOR gates is used for Output Response Analysis (ORA). Simulation of the proposed BIST architecture is carried out in HSPICE using a 45nm CMOS technology, demonstrating 100% fault coverage for single stuck-at faults. The simulation results show a 19% area overhead and a 25% increase in leakage power due to the additional BIST hardware. The area overhead of the proposed BIST-based approach is computed using transistor counting, revealing a 19% increase in the number of transistors in the BIST-included CLBs compared to conventional CLBs.

G. Sudhagar, et. al.[9] Introduced a recursive pseudo-exhaustive two-pattern generator to reduce delays in testing by combining the adder circuit and carry generator. Proposes a two-pattern generator scheme for generic and recursive pseudo-exhaustive testing. Pseudo-exhaustive test pattern generators offer high failure coverage without the need for fault simulation, benefiting from reduced test patterns for combinational faults**.** Recursive pseudo-exhaustive testing proposed in the paper allows for the testing of multiple circuits simultaneously, even with different cone sizes, enhancing efficiency**.** The proposed architecture reduces delays in testing by combining the adder circuit and carry generator into a single block, improving the overall testing process. As the paper addresses, using Built-in Self-Test (BIST) techniques can result in cost savings and effective technical testing procedures for VLSI circuits.

Chioktour V, et. al.[10] Discussed the degradation of the totally self-checking (TSC) property in safety-critical systems due to design issues, crucial for operations like space electronics and medical devices and introduced an adaptive Built-In Self-Test (BIST) unit for concurrent on-line testing on combinational circuits, adjusting input activity to tackle input value absence or low frequency during sleep mode. The proposed architecture uses test vectors as inputs, clusters inputs based on the k-means algorithm, and orders test vectors to minimize subsets, reducing test time significantly. The research explores the impact of low-power techniques on TSC properties using the two-rail checker (TRC) and presents a method to preserve TSC levels while reducing power dissipation in the unit and TSC checker. The study emphasizes the importance of maintaining TSC goals over time, especially when applying low-power techniques that may degrade the TSC property. The paper evaluates the performance of the proposed adaptive BIST unit, showing significant advantages over other solutions for concurrent on-line testing.

H. Xing, et. al.[11] Introduced an approach to high-resolution ADC testing using a digital-compatible BIST strategy, focusing on linearity testing. The research incorporates a low-accuracy thermometer-coded DAC as the MSB array to reduce costs while applying the DDEM method to enhance accuracy, improving the equivalent output linearity of the DAC. The study analytically evaluates the linearity improvement of the DAC and overall testing performance, demonstrating the procedure for measuring specific ADC transition levels under different configurations. By introducing additional linear dither steps using a low-resolution DAC, the work aims to overcome limitations in testing performance due to low-resolution MSB arrays, enhancing the accuracy of ADC testing.

Rashid F, et. al.[12] Explored the use of weighted random patterns (WRP) and transition density patterns (TDP) to reduce test time while maintaining high fault coverage in VLSI circuit testing, by dynamically adapting the scan clock based on transition density, the study shows a significant reduction in test application time without compromising fault coverage, contributing to more efficient testing processes. Transition density patterns (TDP) are highlighted for their potential in
VLSI circuit testing by balancing power consumption, test time, and fault coverage effectively.

Menbari A, et. al. [13] suggested a BIST architecture that can accommodate online and offline testing for

enhancing fault coverage. The findings suggest that TDP can effectively reduce power consumption during testing, offering a practical approach to achieving high-quality tests with reduced test application time and controlled test power. Overall, the paper provides insights into optimizing

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sophisticated contemporary semiconductors. While online BIST employs system input vectors for testing and removes the test pattern generator (TPG) from the chip, offline BIST embeds the TPG in the chip for activation during testing. In order to pass input vectors from a pre-computed test set to the reduction component for testing, the design incorporates a selector module. The test set in the online portion is made up of vectors that, when divided by the polynomial of the LFSR in the selector, yield zero remainders.

A CTL-aware design chooses vectors that, when divided by distinct polynomials, yield the same remainders, hence expanding the size of the test set. The hardware-aware test set with shifted versions of the LFSR's polynomial is used by the internal TPG in the offline section. For effective testing, the reduction section compresses test vector widths and associated outputs. In order to solve the masking issue, a compactor LFSR compresses test vectors to guarantee distinct remainders for every vector. The suggested approach drastically lowers hardware overhead; for large and very large circuits, it is less than 6% and 28%, respectively. According to simulation data, the suggested BIST design performs better in terms of hardware overhead for benchmark circuits such as ISCAS 85, ISCAS 89, and ITC99 than earlier techniques.

Bo, YE, et. al. [14] discussed the new built-in self-test (BIST) structure that is suggested in this study is intended to lower test power dissipation without compromising fault coverage. Test patterns are produced by combining seeds from a modified Linear Feedback Shift Register (LFSR) with a counter and a grey encoder to create single input change patterns. Throughout the course of the 2m test clock period, these test vectors guarantee that each pattern involves a single input change. Through the application of these single input change patterns and the modification of the LFSR to generate seeds, the suggested structure lowers the power consumption without sacrificing fault coverage by substantially reducing the test vectors switching activity during testing. Tests conducted on the ISCAS'89 benchmark circuits demonstrate the efficacy of the new BIST scheme by achieving a significant reduction in power dissipation during testing in addition to providing improved fault coverage.

B. Bhattacharya, et. al. [15] suggested a novel built-in self-test (BIST) scheme to lower energy usage in scan-based circuits, in order to ensure that only valuable patterns are generated in accordance with a predetermined sequence, a mapping logic was constructed to alter the way the circuit generates test patterns. The mapping logic saved energy wasted on pointless patterns by altering the LFSR's state transitions to produce vectors that aid in fault dropping. The suggested solution reduced the amount of energy used in the LFSR during random testing by minimizing the production of unnecessary patterns. Besides, the suggested approach attempted to reduce the amount of energy lost as a result of random switching activity in the circuit and the scan path between applying test vectors. Reducing test application time did not compromise fault coverage, demonstrating the effectiveness of the suggested approach in maximizing energy usage while testing.

Pavlidis A, et. al. [16] discussed about utilizing BIST, more especially the Symmetry-based Built-In Self-Test (SymBIST), which was created initially for testing after production. The study contends that by offering improved insights into circuit behavior and aiding in the resolution of ambiguity groups in defect identification, SymBIST can improve the diagnostic procedure. The study shows that compared to digital circuits, defect diagnostics for analog circuits is far less advanced. Analog ICs still use manual and adhoc procedures, which results in significant ambiguity groups and inefficiencies in problem identification, even though there are many frameworks and tools available for digital IC diagnostics. Within the paper, the application of fault dictionaries is discussed, which associate flaws with diagnostic measurement patterns derived from simulations. Long simulation times are an obstacle to this technology, despite its usefulness. To illustrate the efficacy of the SymBIST technique, the paper presents a case study of a 65nm 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC). The outcomes highlight the potential of BIST in analogue fault identification by showing a notable improvement in defect coverage and diagnosis resolution.

Tang X, et. al. [17] presented a brand-new BIST approach that uses dynamic comparator’s features to identify catastrophic faults. This strategy, in contrast to other approaches that do not consider the particular operational characteristics of dynamic comparators, uses a feedback loop to monitor voltage levels in order to discover errors. The importance of dynamic comparators in high-speed and low-power applications is emphasized in the study. Comprehensive fault diagnosis procedures for dynamic comparators are lacking in the literature, despite the fact that various strategies for checking comparator offsets have been documented. The suggested BIST approach is tested using simulation using HSPICE, Six defective and one fault-free circuit were tested in a ROHM 180nm CMOS and the simulation results of the suggested BIST method, which produced about 87.8% fault coverage with 90 test circuits

V Edward Aliases R, et. al. [18] presented a brand-new TSV BIST technique designed to enhance the identification and fixing of malfunctioning TSVs. This methodology addresses the drawbacks of previous approaches by improving yield and shortening test times. In-depth analysis of the difficulties and procedures involved in testing Through-Silicon Vias (TSVs) in three-

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dimensional integrated circuits (3D ICs) is provided by the author. The study emphasizes how the growing expense and intricacy of sophisticated semiconductor nodes have caused a transition to 3D IC technology. It talks about the different TSV flaws that might happen, like openings, void formations, and shorts, which can have a big effect on the yield of 3D stacked ICs.

The authors stress that a flaw in the TSV could cause the entire 3D IC to be flawed, resulting in higher production costs and worse yields, even if the individual dies are defect-free. The study refers to a number of other investigations that looked at yield loss analysis and cost-saving measures for testing. It does point out, though, that a lot of these methods fall short in addressing the complexity brought about by the clustering of flaws in TSVs. The study presents comprehensive yield analysis and experimental data for a range of chipset designs, showing a notable increase in test efficiency and yield over conventional techniques.

Shaktisinh Jadeja, et. al. [19] demonstrates a number of findings regarding the efficacy of different methods designed to lower power usage during circuit testing. In order to reduce transitions in scan cells, the paper presents three filling strategies: minimum transition filling, 0 filling, and 1 filling. The findings show that these methods can successfully cut down on the number of transitions, which in turn reduces the total amount of power used during testing. This strategy is emphasized as the most successful out of all the ones that have been tried. It maximizes fault coverage while drastically cutting down on power usage. The study suggests that by using this method, problems associated with destructive testing might be reduced, improving production yield and dependability.

5. SUMMARY OF SURVEY

The literature covers a wide range of creative BIST techniques, concentrating on several elements including hardware overhead, fault coverage, power reduction, and testing efficiency. Bo, YE, et al. [14] and Peng Z, et al. [3] both place a strong emphasis on low power usage. Concurrent and adaptive testing with little overhead is the main emphasis of Menbari A, et al. [4] and Menbari A, et al. [13]. Effective pseudo-exhaustive testing is demonstrated by techniques like those outlined by Waller et al. [4] and Sudhagar et al. [9]. Domain-specific advances can be seen in methods for memory testing and particular applications, such as SRAM (Ahmed M. et al. [6]) and high-resolution ADCs (H. Xing et al. [11]). Together, the research improves BIST techniques by maximizing several trade-offs for better VLSI testing.

Table 1. Journal Comparison of Literature survey

Author(s)	Focus	Key Contribution	Results	Advantages
Peng Z, et al.	Low-power test vector generation based on LFSR reseeding.	Optimizes dynamic test power consumption using Hamming distance sorting of test vector seeds.	Reduces test vector seed storage, increases fault coverage, reduces circuit area overhead, and lowers dynamic test power consumption.	Comprehensive benefits in reducing storage bits, minimizing circuit area overhead, and lowering power consumption.
Menbari A, et al.	Concurrent BIST design for concurrent testing during regular operations.	Reduces Concurrent Test Latency (CTL) and minimizes hardware overhead using LFSRs and a minimal decoding module.	Achieves a 10% reduction in hardware overhead and significant CTL reduction for large-scale circuits.	Flexibility to tune hardware overhead and CTL, making it suitable for various applications.
W. Waller, et al.	Algorithm for designing convolved LFSR/SR for pseudo-exhaustive testing.	Minimizes hardware overhead and test set lengths using efficient search algorithms.	New convolved LFSR/SR design (NEWCONV) outperforms existing algorithms in hardware overhead and runtime.	Practical solutions for exhaustive testing with minimal resources.
Ahmed M, et al.	Fault identification and repair in SRAM using BSLFSR and Deep Q-learning.	Combines BSLFSR with DQL for effective fault injection, detection, and repair.	Reduced power consumption and enhanced operating frequency in memory defect recovery.	Outperforms conventional FPGA-based fault detection in terms of size, power consumption, and latency.

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Shrivastava S, et al.	BIST testing techniques for fault detection and coverage.	Evaluates various BIST architectures and proposes a concurrent BIST technique with low hardware overhead.	Successful BIST architecture with minimized slice registers.	Lower hardware overhead compared to other techniques.
Jahanirad H, et al.	BIST for testing LUTs in SRAM-based FPGAs.	Uses a 4-bit counter and XOR gates for output response analysis.	100% fault coverage for single stuck-at faults, with a 19% area overhead and 25% increase in leakage power.	Effective fault coverage with moderate area and power overhead.
Kumar M, et al.	Memory testing in SOC designs, including BISD schemes.	BIST structure capable of detecting and diagnosing faults in interconnects and CLBs.	Enhances memory yield and effective testing of non-volatile memory failures.	Effective diagnosis of multiple fault types.
Chioktour V, et al.	Adaptive BIST unit for concurrent on-line testing in safety-critical systems	Test vectors using k-means clustering to minimize subsets, preserving TSC properties.	Showed significant advantages over other solutions for concurrent on-line testing.	Significant reduction in test time and maintenance of TSC goals while reducing power dissipation.
H. Xing, et al.	High-resolution ADC testing using a digital-compatible BIST strategy.	Low-accuracy thermometer-coded DAC for linearity testing and DDEM method for accuracy improvement.	Demonstrated improved linearity and overall testing performance.	Enhanced accuracy and cost reduction in ADC testing.
Rashid F, et al.	Use of WRPs and TDPs to reduce test time while maintaining high fault coverage.	Dynamic adaptation of scan clock based on transition density.	Effective balancing of power consumption, test time, and fault coverage.	Significant reduction in test application time and power consumption.
Bo, YE, et al.	BIST structure to lower test power dissipation.	Single input change patterns and modified LFSR for reduced switching activity.	Significant reduction in power dissipation and improved fault coverage.	Lower power consumption without sacrificing fault coverage
B. Bhattacharya, et al.	BIST scheme to lower energy usage in scan-based circuits.	Mapping logic to alter LFSR state transitions and produce valuable test patterns.	Demonstrated effectiveness in maximizing energy usage during testing.	Reduced energy consumption and test application time without compromising fault coverage.

6. CONCLUSION

This review has given a thorough overview of methods for improving the efficiency of Built-In Self-Test (BIST) approaches used in VLSI (Very Large-Scale Integration) testing. This article emphasizes how BIST is always developing and finding new uses in VLSI and System-on-Chip (SoC) testing. This progression highlights the increasing significance of BIST for thorough defect detection, demonstrating its flexibility and applicability in modern electronic testing settings. According to the survey, in order to stay up with the rapid improvements in VLSI technology, continuous research and development in BIST techniques is vital. Future developments in this area depend heavily on the integration of advanced test pattern generation and analysis techniques, the design of effective BIST controllers, and ongoing innovation in test power reduction.

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BIOGRAPHIES AND PHOTOGRAPHS

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