Int. J. Advanced Networking and Applications
Volume: 03, Issue: 01, Pages:1031-1034 (2011)

Pipelined C^2Mos Register High Speed Modified Booth Multiplier.

N.Ravi
Department of Physics & Electronics, RGM Engg College,
JNT University, Anantapur, Andhra Pradeh-518501
Email: ravi2728@gmail.com
Dr.T.Subba Rao
Professor, Department of Physics,
Sri Krishnadevaraya University, Anantapur, Andhra Pradesh-515003.
Email: sushmasurekha@yahoo.co.in
Dr.T.Jayachandra Prasad
Professor, Department of ECE, RGM Engg College,
JNT University, Anantapur, Andhra Pradeh-518501
Email: jp.talari@gmail.com

----------ABSTRACT----------

This paper presents C^2Mos register Pipelined Modified Booth Multiplier (PMBM) to improve the speed of the multiplier by allowing the data parallel. The pipeline registers are designed with two p-mos and two n-mos transistors in series which is C^2Mos. Wallace multiplier also used to improve the speed of the multiplier with Carry Save Addition. 16-Transitor Full adders are used for better performance of the multiplier. The PMBM is 28.51% more speed than the Modified Booth Multiplier (MBM). This is calculated with TSMC 0.18um technology using Hspice.

Keywords- **Modified Booth Multiplier, Pipeline, Register, Wallace Tree.**

Date of submission: April 19, 2011 Date of Acceptance: June 01, 2011

I. INTRODUCTION

Multiplication and multiplication-accumulation (MAC) are very common mathematical operations in many Digital Signal Processing (DSP) applications. There are three major steps to any multiplication. In the first step, the partial products are generated. In the second step, the partial products are reduced to one row of final sums and one row of carries. In the third step, the final sums and carries are added to generate the result [1-3].For high speed DSP applications Booth multiplier is used, in which N number of partial products can be halved. Hence the hardware of the multiplier will be reduced which will increase its performance.

Low latency demands high performance circuitry, and small physical size to limit propagation delays. VLSI implementations are the only available means for meeting these two requirements, but efficient algorithms are also crucial. An extension to Booth's algorithm for multiplication has been developed, which represents partial products in a partially redundant form. This redundant representation can reduce or eliminate the time required to produce "hard" multiples required by the traditional higher order Booth algorithms. This extension reduces the area and power requirements of fully parallel implementations, but is also as fast as any multiplication method yet reported.

In Section-II the mathematical expression for Booth multiplier and Modified Booth Multiplier is given. The efficient encoder and decoder circuits are also shown. The Section-II deals with Wallace Tree multiplier for the improvement of the multiplier. Pipeline technique is explained in Section-IV. Results and discussions are discussed in Section-V. Finally, the main conclusions of the paper are summarized in Section VI.

II. BOOTH MULTIPLIER

1. CONVENTIONAL BOOTH MULTIPLIER

Consider the multiplication of two n-bit integer numbers A (multiplicand) and B (multiplier) in 2's compliment representation, i.e.,

$$A = -a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i$$

$$B = -b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i \qquad (1)$$

Volume: 03, Issue: 01, Pages:1031-1034 (2011)

2. MODIFIED BOOTH (Radix-4) MULTIPLIER

Modified Booth Recoding algorithm [8] is one of the most popular techniques to reduce the number of partial products to be added while multiplying two numbers. Reduction in number of partial products depends upon how many bits are recoded. If 3-bit recoding (Radix-4) is used the number of partial products is reduced by half.
In MBE, B in (1) becomes

$$B = \sum_{i=0}^{n/2-1} m_i 2^{2i} = \sum_{i=0}^{n/2-1} (-2b_{2i+1} + b_{2i} + b_{2i-1}) 2^{2i} \quad (2)$$

where $b-1 = 0$, and $m_i \in \{-2,-1, 0, 1, 2\}$. According to the encoded results from B, the Booth selectors choose $-2A$, $-A$, 0, A, or $2A$ to generate the partial product rows, as shown in Table I. The $2A$ in Table I is obtained by left shifting A one bit. The encoder and decoder circuits are shown in "Fig. 1."Negation operation is achieved by complementing each bit of A (one's complement) and adding "1" to the least significant bit. Adding "1" is implemented as a correction bit *neg*, which implies that the partial product row is negative (*neg* = 1) or positive (*neg* = 0). In addition, because partial product rows are represented in 2's complement representation and every row is left shifted two bit positions with respect to the previous row, sign extensions are required to align the most significant parts of partial product rows. These extra sign bits will significantly complicate the reduction tree. Therefore, many sign extension schemes [4]–[7] have been proposed to prevent extending up the sign bit of each row to the $(2n - 1)$th bit position.

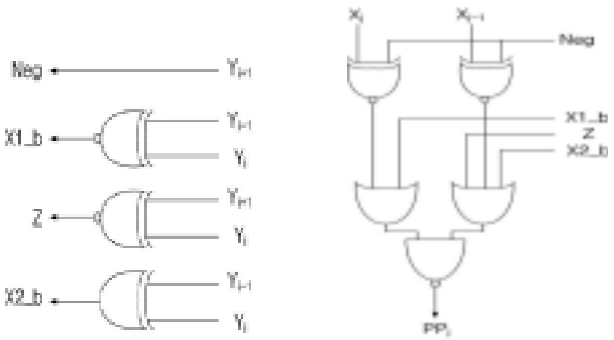

Fig. 1. i) Encoder circuit ii) Decoder circuit

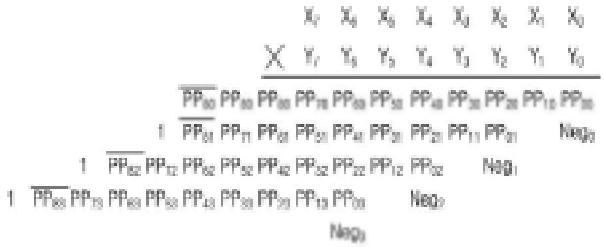
Fig. 2. Multiplication method

TABLE .I. TRUTH TABLE OF MBE SCHEME

Y_{i-1}	Y_i	Y_{i+1}	Value	X_{1_b}	X_{2_b}	Neg	Z
0	0	0	0	1	0	0	1
0	0	1	1	0	1	0	1
0	1	0	1	0	1	0	0
0	1	1	2	1	0	0	0
1	0	0	-2	1	0	1	0
1	0	1	-1	0	1	1	0
1	1	0	-1	0	1	1	1
1	1	1	0	1	0	1	1

III. WALLACE TREE MULTIPLIER

The Wallace tree shows a good performance by using the carry save adders instead of the ripple carry adders. It is, however, still the most critical part of the multiplier because it is responsible for the largest amount of computation. Wallace introduced a different way of parallel addition of the partial product bits using a tree of carry save adders, which is known as "Wallace Tree". In order to perform the multiplication of two numbers with the Wallace method, partial product matrix is reduced to a two-row matrix by using a carry save adder and the remaining two rows are summed using a fast carry-propagate adder to form the product. This Wallace method can be used.

CSA performs the addition of m numbers in lesser duration compared to the simple addition. It takes three numbers (a+b+c) to add together and outputs two numbers, sum and carry (s+c).It is carried out in one time unit duration .In carry –save adder, the carry(c) is bought until the last step and the ordinary addition carried out in the very last step . The most important application of a carry-save adder is to calculate the partial products in integer multiplication. This allows for architectures, where a tree of carry save adders (also called *Wallace tree*) is used to calculate the partial products very fast. One 'normal' adder is then used to add the last set of carry bits to the last partial products to give the final multiplication result. Usually, a very fast carry-look ahead or carry-select adder is used for this last stage, in order to obtain the optimal performance [9].

Volume: 03, Issue: 01, Pages:1031-1034 (2011)

IV. PIPELINE TECHNIQUE

The pipelining is a popular technique to increase throughput of a high speed system, which divides total system into several small cascade stages and adds some registers to synchronize outputs of each stage. Also parallel-pipeline architecture is considered to be most suitable for low voltage and low power systems [10, 11]. In a pipelining system, the maximum operating frequency is limited by the slowest stage which has the longest delay time. C^2 Mos D-Flip Flops shown in "Fig.3." are used in the pipeline stages for parallel processing the data. The pipelines are used at input and output stages of the Wallace multiplier. The non pipelined structure of the Modified Booth Multiplier is shown in "Fig. 4." The pipelined structure of the MBM is shown in "Fig. 5."

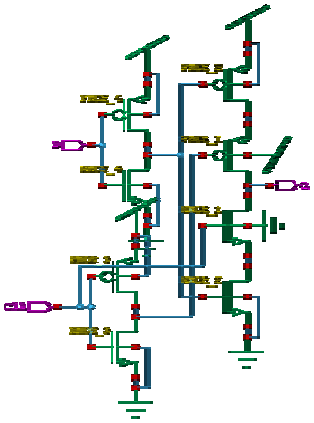

Fig. 3. C^2Mos-Register

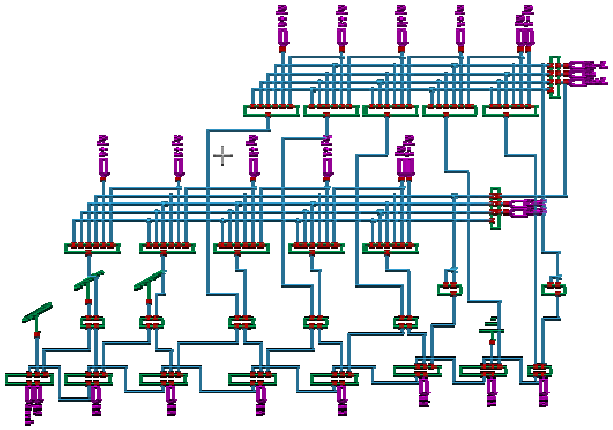

Fig. 4. The design of the MBE

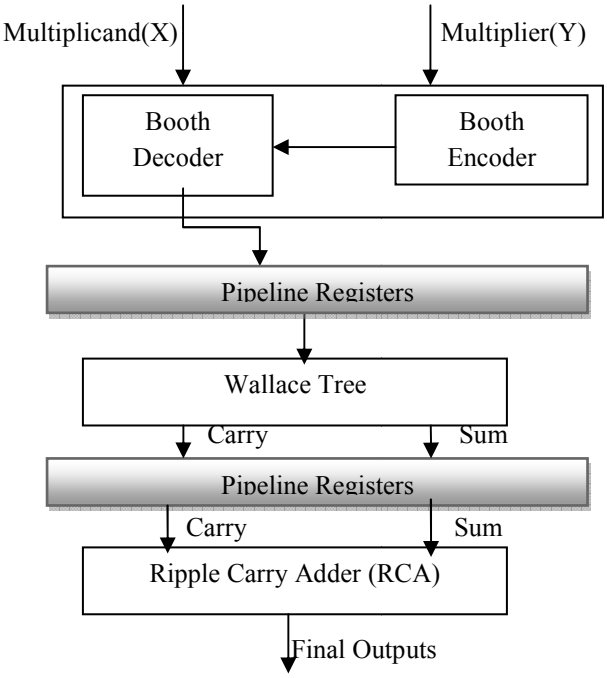

Fig. 5. Architecture of the PMBM

V. RESULTS AND DESCUSSION

The Modified Booth Multiplier (MBM) is simulated with TSMC 0.18um technology using Hspice. The propagation delays of all inputs and outputs are calculated. To show the MBM very good performance the Wallace Tree Full adders are constructed with 16-Transistors. The performance of the 16-T full adder is as shown in "Table. II." Among them the longest delay i.e worst case delay is given in the "Table. III." In 8x8 MBM the Pipelined multiplier is 28.51% more speed compared to non-pipelined multiplier for that technology. The number of transistors in the MBM is 1618 and in PMBM is 3984. The difference is 2366 due to pipelined C^2Mos registers. These registers also cause to consume 50.92% more power. The pipelined multiplier is aimed for speed not on power. The dynamic, RMS and Maximum power of the PMBM is less compared to MBM. The short circuit power and leakage power is more for PMBM than that of the MBM. MBM also designed with Carry Look ahead Adder (CLA) results shown in the "Table. III".

TABLE.II. POWER, DELAY AND ENERGY CONSUMPTION OF THE 16-T ADDER.

Technology at (25^0C)	16-T Full-Total Power	16-T Full-Prop-Delay	EDP (JS)
0.18um	8.88E-06	5.08E-10	2.29161E-24
90nm	1.36E-05	5.07E-10	3.49587E-24
65nm	6.15E-06	5.06E-10	1.57462E-24

TABLE.III. PERFORMANCE COMPARISION OF THE MODIFIED BOOTH MULTIPLIER

Multiplier	Total Power	Dynamic Power	RMS Power	Prop-Delay	Max Power	No.of Transistors
8x8(RCA)	1.6671E-02	44.8474u	3.5192E-02	1.4052E-09	1.1891E-01	1618
8x8(Pipe-RCA)	2.1763E-02	719.08n	3.7198E-02	1.0045E-09	1.1724E-01	3984
8x8(CLA)	1.6341E-03	1.0711m	3.2669E-03	2.5899E-10	4.7641E-02	2062

VI. CONCLUSION

This paper described the Pipelined Modified Booth Multiplier for high speed applications. Due to N number of partial product reduction in Booth Multiplier into N/2, it reduces number of gate delays then shows high speed. Pipelined technique is used to create small delay in input then allowing all the input at the same time. The PMBM shown 28.51% more speed than Non Pipelined Booth Multiplier. The well structured C^2Mos registers shown more performance of the multiplier. In this paper the PMBM is designed with Ripple Carry Adder (RCA). So this multiplier also shows performance in power due RCA.

REFERENCES

[1] V. G. Oklobdzija, D. Villeger, and S. Liu, A Method for Speed Optimized partial product Reduction and Generation of Fast Parallel Multipliers Using an Algorithmic Approach, *IEEE Trans. Computers*, *vol. 45*, p.p. 294-306, 1996.

[2] S. Hsu, et al, A 110GOPS/W 16b Multiplier and Reconfigurable PLA Loop in 90nm CMOS, *IEEE ISSCC Dig. Tech. Papers*, pp. 376-377, 2005.

[3] W. C. Yeh and C. W. Jen, High-Speed Booth Encoded Parallel Multiplier Design, *IEEE Trans. Computers*, *vol. 49,* p.p. 692-701, 2000.

[4] J. Fadavi-Ardekani, *M* × *N* booth encoded multiplier generator using optimized Wallace trees, *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 1, no. 2, pp. 120–125, Jun. 1993.

[5] O. Salomon, J.-M. Green, and H. Klar, General algorithms for a simplified addition of 2's complement numbers, *IEEE J. Solid-State Circuits*, vol. 30, no. 7, pp. 839–844, Jul. 1995.

[6] E. de Angel and E. E. Swartzlander, Jr., Low power parallel multipliers, in *Workshop VLSI Signal Process. IX*, 1996, pp. 199–208.

[7] A. A. Farooqui and V. G. Oklobdzija, General data–path organization of a MAC unit for VLSI implementation of DSP processors, in *Proc. IEEE Int. Symp. Circuits Syst.*, 1998, vol. 2, pp. 260–263.

[8] A.D.Booth, **A** signed binary multiplication technique, *Quart. J. Math., vol. IV*, pt. 2, 1951.

[9] Behrooz parahmi, Computer Arithmetic: Algorithms and Hardware Design*s*, *Oxford University Press,* 2000.

[10] A. P. Chandrakasan, S. Sheng, R. W.Broderson, Low Power CMOS Digital Design, *IEEE J. Solid-state Circuits*, *Vol. 27, No. 4*, 1992, pp. 473-483.

[11] A. P. Chandrakasan, R. W. Broderson*,* Minimizing Power Consumption in Digital CMOS Circuits*,* Proc. IEEE, Vol . 83, No. 84, 1995, pp. 498-523.

Authors Biography

N.Ravi holds B.Sc degree in electronics at Osmania Degree College-Kurnool, S.K. University, Anantapur, Andhra Pradesh-India in 1998. He obtained Masters Degree in Physics (Solid State Physics) at S.K.University, Anantapur, AP- India in 2001. He is pursuing Ph.D in VLSI Design from Sri Venkateswara University, Tirupati. He is presently working at Rajeev Gandhi memorial College of Engg & Technology, Nandyal, Andhra Pradesh-India as an Assistant professor in the department of Physics. His area of interest includes Low Power VLSI Design, FPGA, Solid State Physics and Nanotechnology.

Dr.T.Subba Rao is a Professor in the department of Physics, Sri Krishnadevaraya University, Anantapur, Andhra Pradesh-India.

Dr.T.Jayachandra Prasad is a Principal and Professor of ECE at Rajeev Gandhi Memorial College of Engg & Technology, Nandyal, Andhra Padesh-India