Design, Implementation and comparison of 8-Bit Vedic Multiplier Using Multiplexers and Logic Gates

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ABSTRACT- In this paper, the design of high speed 8-bit vedic multiplier using multiplexers is presented. Vedic mathematic is the ancient Indian system of mathematics. It is mainly based on 16 sutras. In that 14th sutra is Urdhva Tiryakbhyam sutra which means vertical and crosswise. This sutra is used for designing of vedic multiplier in that the first design involves implementation of 8-bit Vedic multiplier using basic gates and the second design involves implementation of high speed 8-bit Vedic multiplier by using multiplexers. The system is designed using VHDL and it is implemented through Xilinx ISE 14.5.

Keywords— *Multiplier, Vedic multiplier, Vedic Mathematics, Urdhava Triyagbhyam*.

I. INTRODUCTION

Vedic mathematics is an ancient Indian system of mathematics consists of Vedic sutras .Vedic mathematics gives a simplified and optimized solutions compare to the conventional mathematical algorithms.

This Vedic algorithm are applied to a several mathematical operations [1] such as arithmetic, trigonometric, geometric operations in that one such operation is Vedic multiplier which is used for digital multiplier in digital signal processing applications.

Vedic mathematics consists of 16 sutras [2] which covers whole mathematical operations and digital multiplier based on Vedic multiplier are the fastest, reliable, efficient and low power multipliers by reducing the number partial products the delay also decreased and the system becomes faster.

From 16 sutras the 14th sutra is Urdhva Tiryakbhyam sutra Which is related for multiplication operation and this sutra is best suitable for lesser magnitude values.

II. URDHVA TIRYAKBHYAM SUTRA

In Urdhva Tiryakbhyam sutra operation are performed in vertical and crosswise manner. Multiplication operation is done by simple addition of partial products. In this sutra the parallelism architecture is used which means generation of partial products and their summing is performed simultaneously. As a result processor speed increases, calculations of Urdhva Tiryakbhyam sutra is shown in fig. 1.

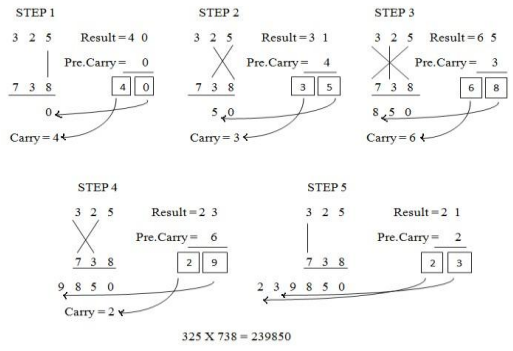


Fig.1: Multiplication of two decimal numbers by Urdhva Tiryakbhyam

Multiplication of two numbers 325x738 is performed by vertical and crosswise manner ,the result obtained by this multiplication is added with the carry generated from every pervious step and the procedure is continued till last bit of the input

III. 8-BIT VEDIC MULTIPLIER

The existing 8-bit vedic multiplier consists of four 4-bit vedic multipliers and three 8- bit ripple carry adder. Let us take A and B are of 8-bit input which gives an output S of sixteen bit and results are obtained after getting partial product and doing addition. Fig. 2 shows an existing 8-bit vedic multiplier.

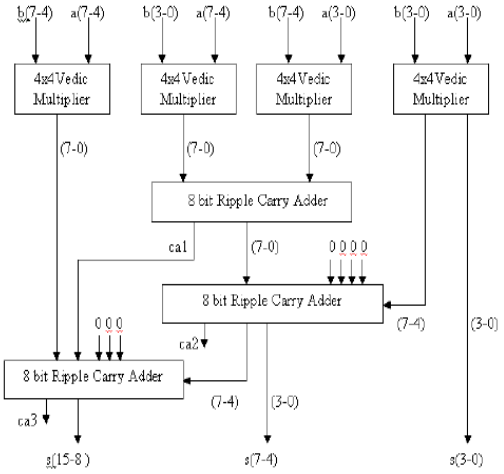


Fig.2: 8-bit Vedic multiplier

8-BIT VEDIC MULTIPLIER USING BASIC GATES:

The 8-bit vedic multiplier architecture is implemented by using logic gates, steps involved in implementation of vedic multiplier is first the design of 2-bit Vedic multiplier and second the design of 4-bit vedic multiplier for this four 2-bit vedic multiplier is used and they are interconnected by ripple carry adders. By using logic gates 2-bit vedic multiplier is shown in Fig.3

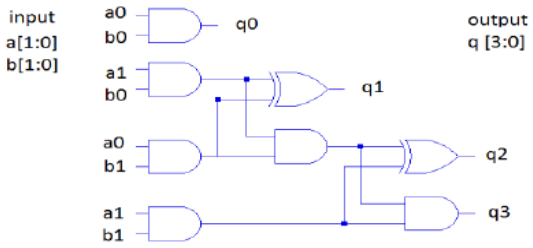


Fig.3: 2-bit Vedic multiplier using logic gates .

Let us take A and B are of 2-bit input which gives an output S of 4-bits , summing of partial products is performed by half adders same procedure is used in designing of 4-bit vedic multiplier in place of half adders ripple carry adders are used and is shown in Fig.2

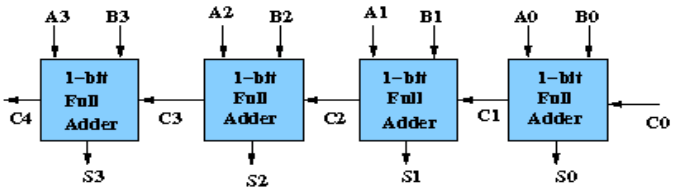


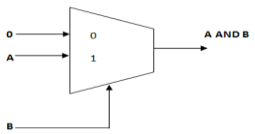
Fig.4: 4-bit ripple carry adder

The ripple carry adder consists of 2 inputs A and B of 4-bit and carry C of previous adder and produces an output S of 4-bits. By using two, four bit vedic multiplier and 8-bit ripple carry adder an 8-bit Vedic multiplier is designed as shown in Fig.4.

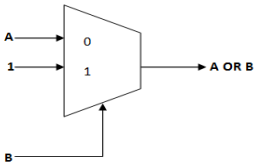
IV. 8-BIT VEDIC MULTIPLIER USING MULTIPLEXERS

The 8-bit vedic multiplier architecture is implemented by using multiplexers, all logic gates are replaced by multiplexers. Design of some of the basic gates by using multiplexers is shown.

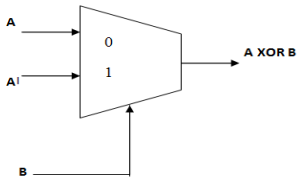
i. AND gate using multiplexer



ii. OR gate using multiplexer



iii. XOR gate using multiplexer



By using these multiplexers 2-bit vedic multiplier using multiplexers is designed by replacing AND, OR, and XOR gates by multiplexers is shown in Fig.5.

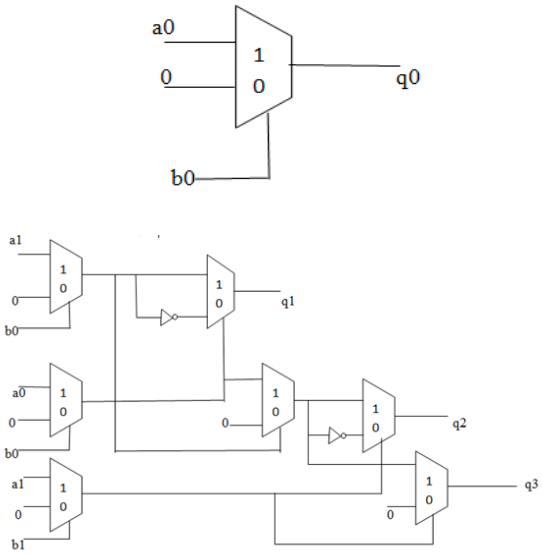


Fig.5: 2-bit Vedic multiplier using multiplexers.

Take _a_ and ' b' are of 2-bit input which gives an output _q' of 4-bits here all the logic gates are replaced by multiplexers and summing of partial products is performed by half adders these adders also replaced by logic gates same procedure is used in designing of 4-bit Vedic multiplier in place of half adders ripple carry adders are used and they also replaced by multiplexers. By using two, four bit Vedic multiplier and 8-bit ripple carry adder using multiplexers an

8-bit Vedic multiplier using multiplexers is designed as shown in Fig.2.

V. SIMULATION RESULTS

The proposed 8-bit Vedic multiplier is coded in VHDL, simulated using Xilinx ISim simulator, synthesized using Xilinx XST and verified for the inputs a=00000011 and b=00000001which gives output of s=0000000000000011. The RTL schematic and simulation results of 8-bit Vedic multiplier are shown in Fig.6 and Fig.7.

Fig.6: Simulation results of 8x8 Vedic multiplier using multiplexers.

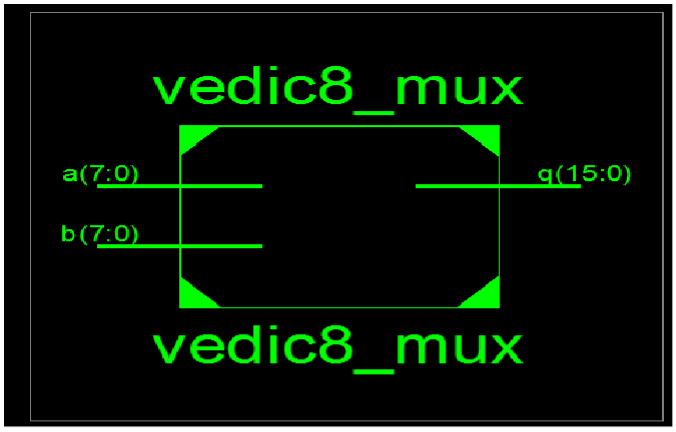


Fig.7: RTL diagram of 8x8 Vedic multiplier using multiplexers

Device utilization summary

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Device utilization summary:
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Selected Device : 6slx45csg324-3


Slice Logic Utilization:
 Number of Slice LUTs:                  26  out of  27288     0%
    Number used as Logic:               26  out of  27288     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    26
   Number with an unused Flip Flop:     26  out of     26   100%
   Number with an unused LUT:            0  out of     26     0%
   Number of fully used LUT-FF pairs:    0  out of     26     0%
   Number of unique control sets:        0

IO Utilization:
 Number of IOs:                         16
 Number of bonded IOBs:                 16  out of    218     7%
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Total REAL time to Xst completion: 6.00 secs
Total CPU time to Xst completion: 6.12 secs

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Total memory usage is 186496 kilobytes
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Timing Detail

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All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 536 / 8
-------------------------------------------------------------------------
Delay:               10.211ns (Levels of Logic = 7)
  Source:            a<0> (PAD)
  Destination:       q<6> (PAD)

  Data Path: a<0> to q<6>
                                   Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             10   1.222   1.104  a_0_IBUF (a_0_IBUF)
     LUT4:I0->O             4   0.203   0.931  v2/x1/m1/Mmux_o111 (q2<1>)
     LUT6:I2->O             2   0.203   0.845  Fa1/a3/m7/m1/Mmux_o111 (Fa1/ca3)
     LUT5:I2->O             2   0.205   0.981  Fa2/a4/m2/m1/Mmux_o111 (out2<3>)
     LUT6:I0->O             2   0.203   0.961  Fa3/a2/m7/m1/Mmux_o111 (Fa3/ca2)
     LUT5:I0->O             1   0.203   0.579  Fa3/a3/m2/m1/Mmux_o111 (q_6_OBUF)
     OBUF:I->O                  2.571          q_6_OBUF (q<6>)
    ----------------------------------------
    Total                      10.211ns (4.810ns logic, 5.401ns route)
                                        (47.1% logic, 52.9% route)

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Table-1: Comparison between Vedic multipliers using basic gates and multiplexers.

Multiplier type	Vedic multiplier using basic gates	Vedic multiplier using multiplexers
Total Delay(ns)	17.102	10.211
Logic Delay(ns)	6.032	4.810
Route Delay(ns)	11.070	5.401
Total memory usage	196980 kilobytes	186496 kilobytes
Logic Levels	13	7

The8-bit vedic multiplier using multiplexers designed and compared with 8-bit vedic multiplier using basic gates in terms of total delay, logic delay ,route delay, total memory usage and number of logic levels .The results are tabulated in table 1 and it shows that there is a reduction in total delay, logic levels and memory usage. Thus, the proposed design is more efficient than the Vedic multiplier using basic gates.

VI. CONCLUSION

The 8-bitVedic multiplier architecture using multiplexers are designed by using Urdhva tiryagbhyam sutra. The total delay, memory usage and logic levels are reduced when compared with the design of vedic multiplier using basic gates.

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